

**TIERED MULTI-MEDIA ACCELERATION SCHEDULER ARCHITECTURE
FOR DYNAMIC CONFIGURABLE DEVICES**

ABSTRACT OF THE DISCLOSURE

Disclosed is a device architecture for running applications. The device architecture includes an operating system (OS) having an OS scheduler, a Dynamic Configurable Hardware Logic (DCHL) layer having a plurality of Logic Elements (LEs) and, interposed between the OS and the DCHL layer, a TiEred Multi-media Acceleration Scheduler (TEMAS) that cooperates with the OS scheduler for scheduling and configuring the LEs of the DCHL to execute applications. In the preferred embodiment the TEMAS is constructed to contain a Tier-1 scheduler that communicates with the OS scheduler, and at least one Tier-2 scheduler interposed between the Tier-1 scheduler and one DCHL configurable device.